Reg. No: ☐☐☐☐☐☐☐☐☐☐

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech III Year II Semester Regular & Supplementary Examinations October-2020
DIGITAL IC APPLICATIONS
(Electronics & Communication Engineering)

Time: 3 hours   Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1 **a** Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation.   **7M**

b Explain TTL and CMOS interfacing.   **5M**

OR

2 **a** Design CMOS transistor circuit for 2-input AND gate. With the help of function table, explain the circuit   **6M**

b Design a CMOS circuit that has the functional behavior f(Z)=A.(B+C).   **6M**

UNIT-II

3 Design the logic circuit and write VHDL program for the following functions

a F(X) = ΣA, B, C, D (0, 2, 5, 7, 8, 10, 13, 15) + d (1, 6, 11).   **6M**

b F(Y) = ΠA, B, C, D (1, 4, 5, 7, 9, 11, 12, 13, 15).   **6M**

OR

4 **a** What is the importance of time dimension in VHDL and explain   **6M**

b Explain the behavioral design elements of VHDL.   **6M**

UNIT-III

5 **a** Write a VHDL code for 4-bit ALU IC 74x181.   **6M**

b Draw the structure of a 4-bit comparator and briefly explain about it. Write a structural VHDL code for it.   **6M**

OR

6 **a** Design a Full adder with Half adders logic circuit.   **6M**

b Write VHDL code for the above design in structural model.   **6M**

UNIT-IV

7 **a** Draw the standard IC diagram of 74x194 and explain its operation. Write VHDL code for 74X194.   **8M**

b What do you mean by self-correcting counter.   **4M**

OR

8 **a** Design a 4-bit Johnson Counter and explain its operation.   **6M**

b Write a VHDL code for the above design.   **6M**

UNIT-V

9 **a** Distinguish between the synchronous and asynchronous counters.   **6M**

b What are the impediments to synchronous design?   **6M**

OR

10 **a** Design an 8 bit serial in and parallel out shift register.   **6M**

b Design a decade counter and explain its operation with necessary waveforms.   **6M**

*** END ***